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6	CPU-Power
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11	PCH-SATA/HOST/GPIO/DDI/VGA
12	PCH-SMB/LPC/AUDIO/RTC
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14	PCH-GND
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CPU :

Intel Haswell Processor

System Chipset :

Intel Lynx Point Chipset

On Board Chipset :

**VRM 12.5 -- NCP81102+NCP81161 4Phase
Gigabit LAN -- RTL8111GN Co-lay RTL8111F-VB
HDA Codec -- Realtek ALC892 Co-lay ALC662-VD
Super I/O -- NCT5533D
SPI Flash 64Mb+16Mb**


Main Memory :

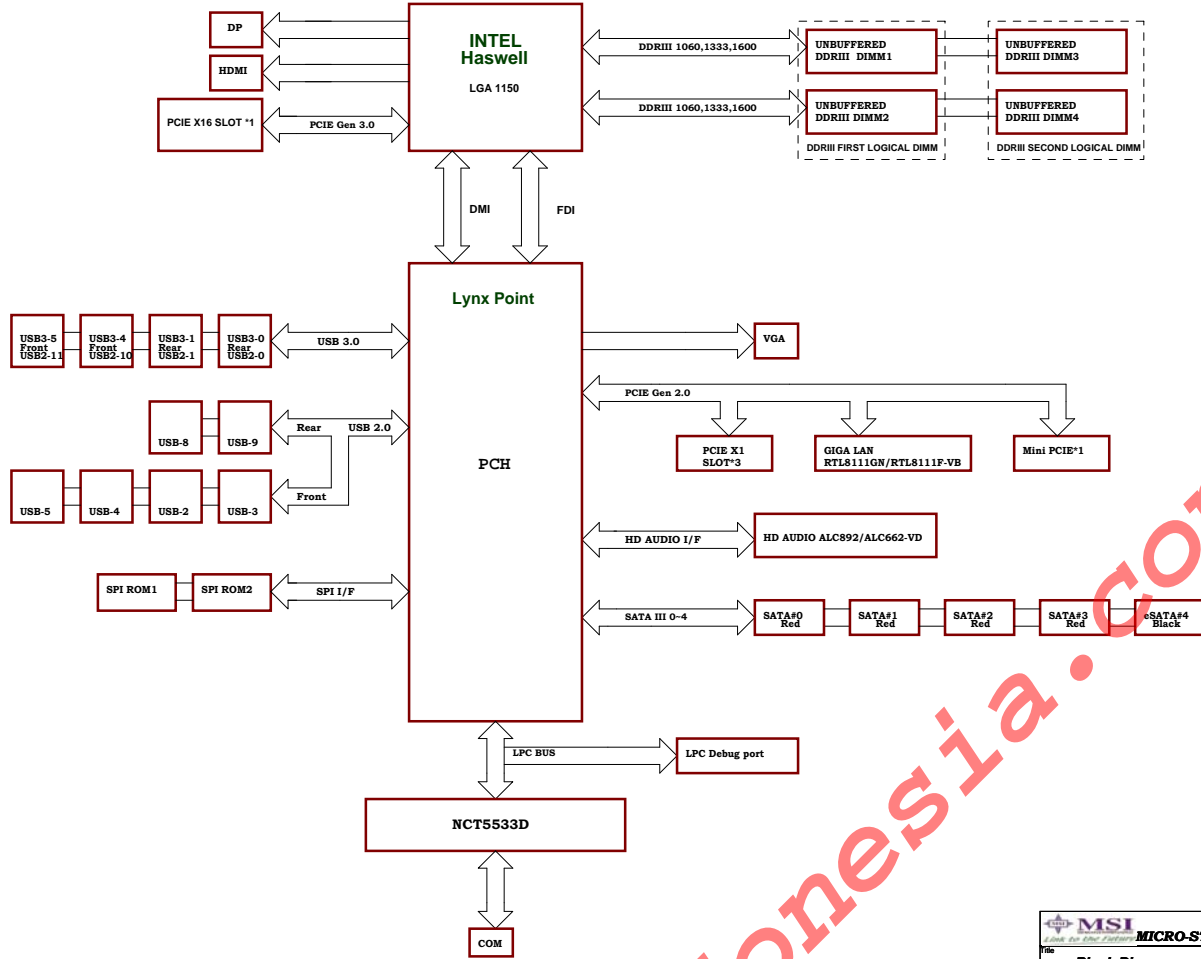
2 Channel DDR III * 4 (Max 32GB)

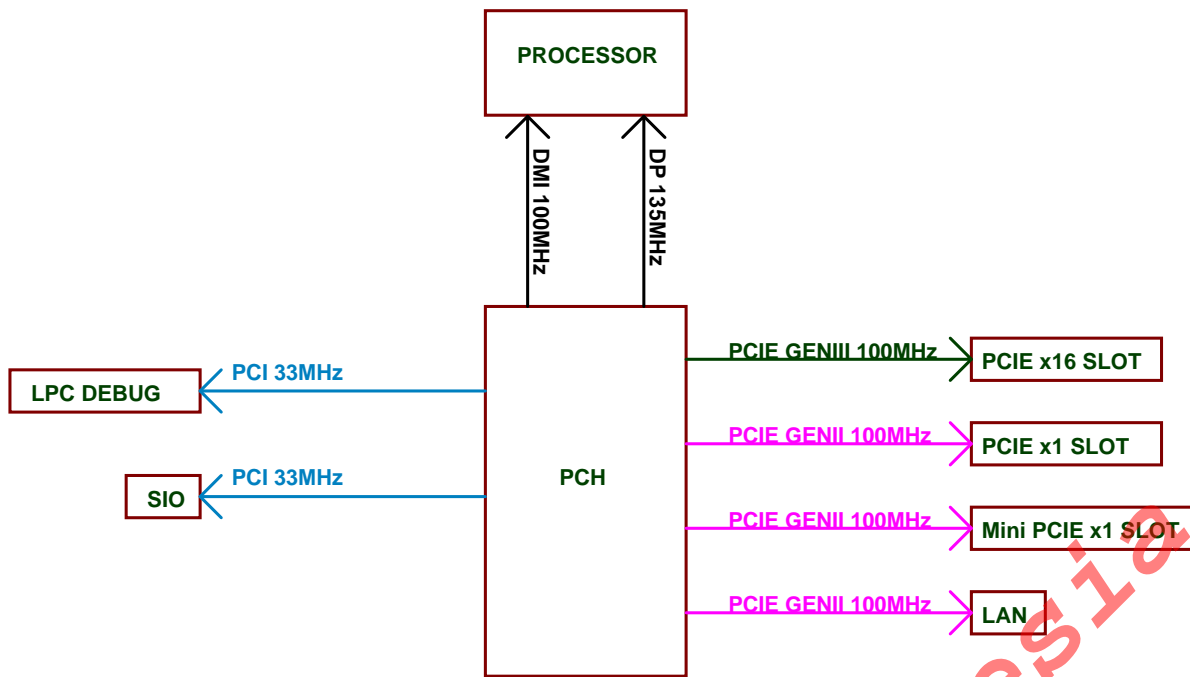
Expansion Slot :

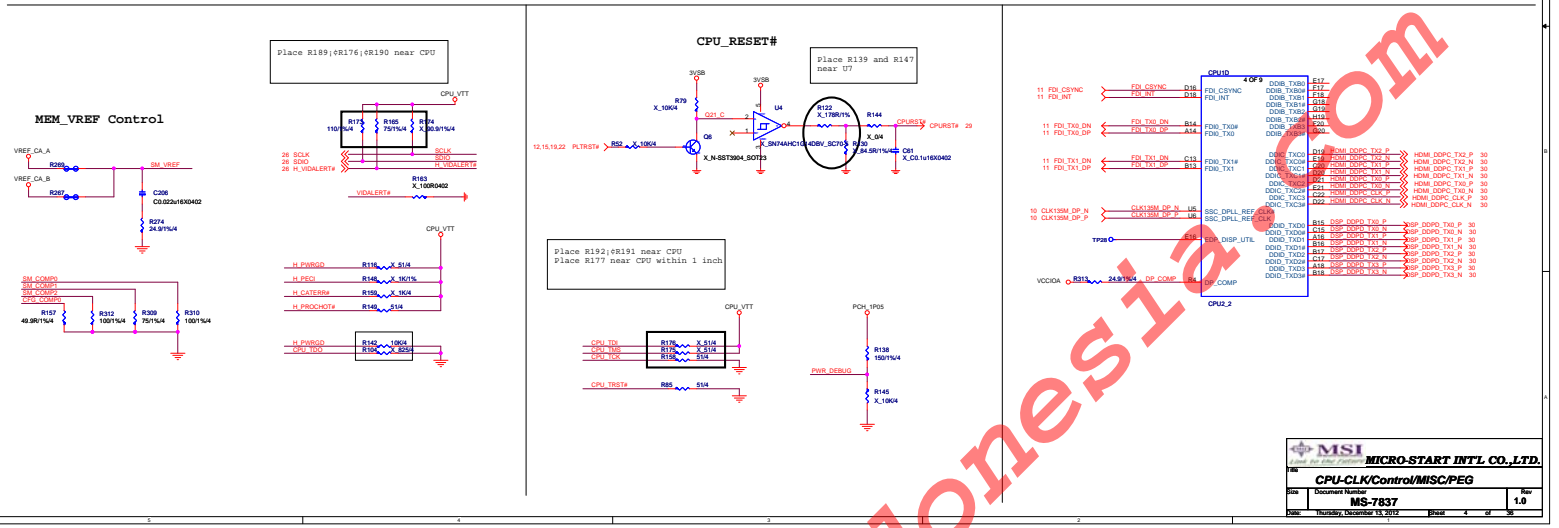
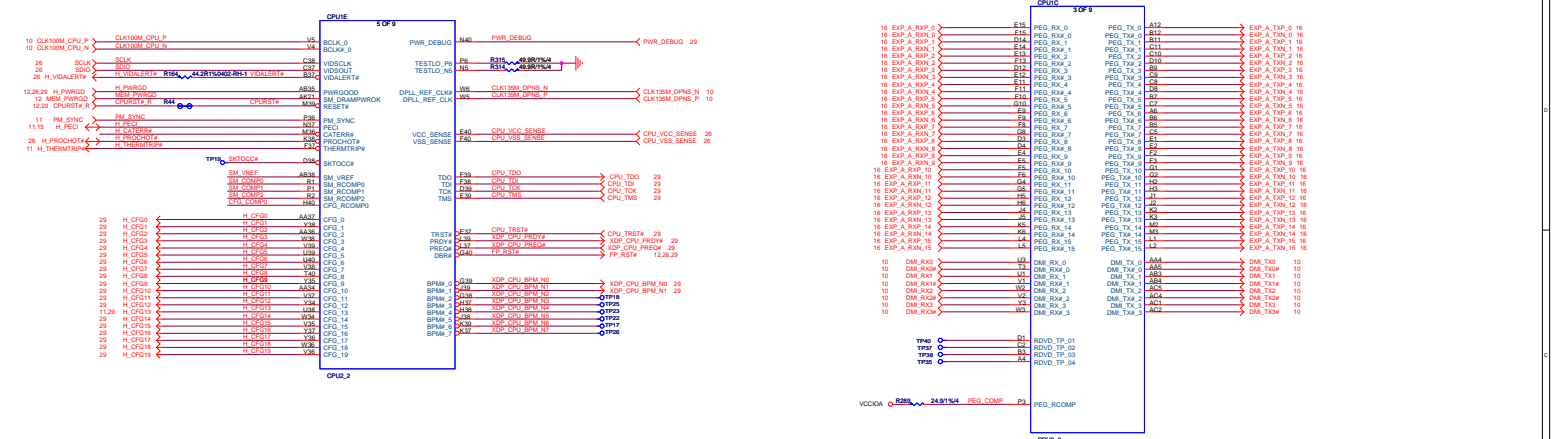
**PCI Express x16 Slot * 1
PCI Express x1 Slot * 3
Mini PCIE/Mini SATA Slot * 1**

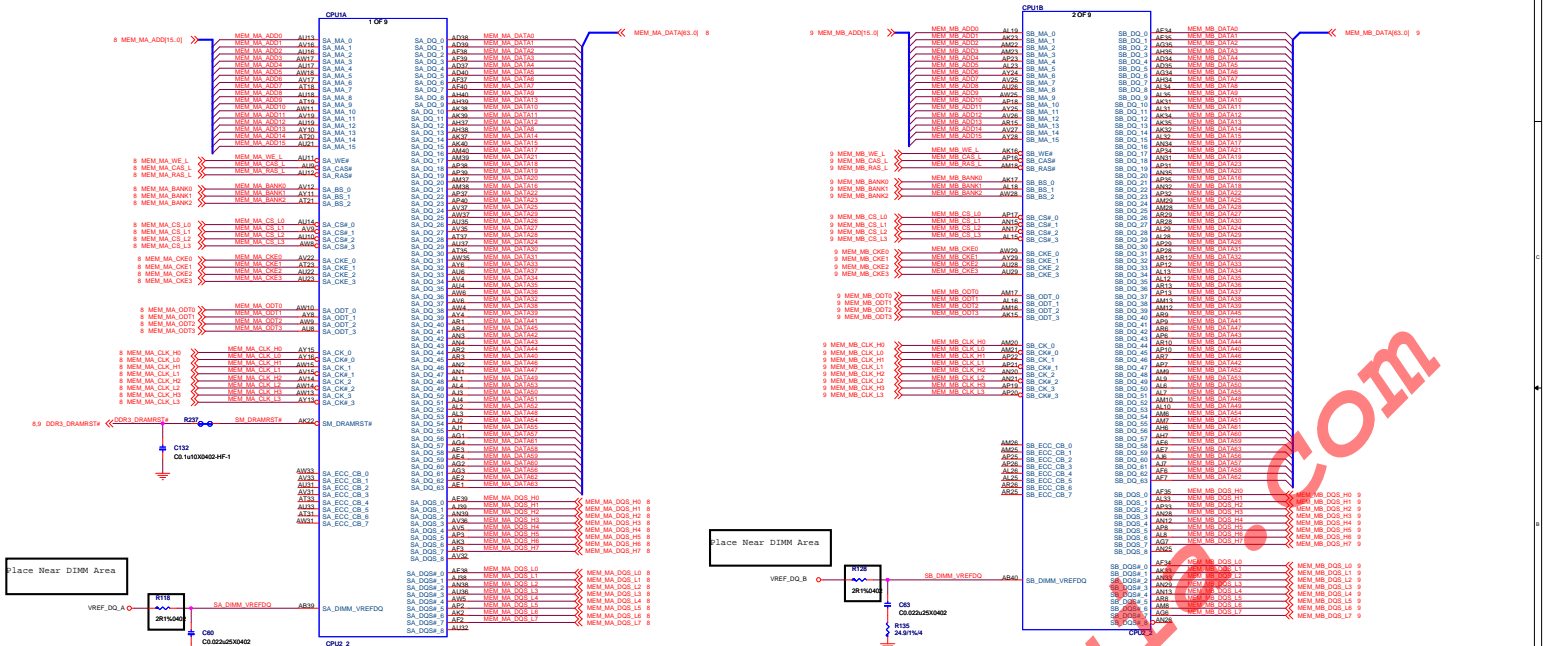
lenovo

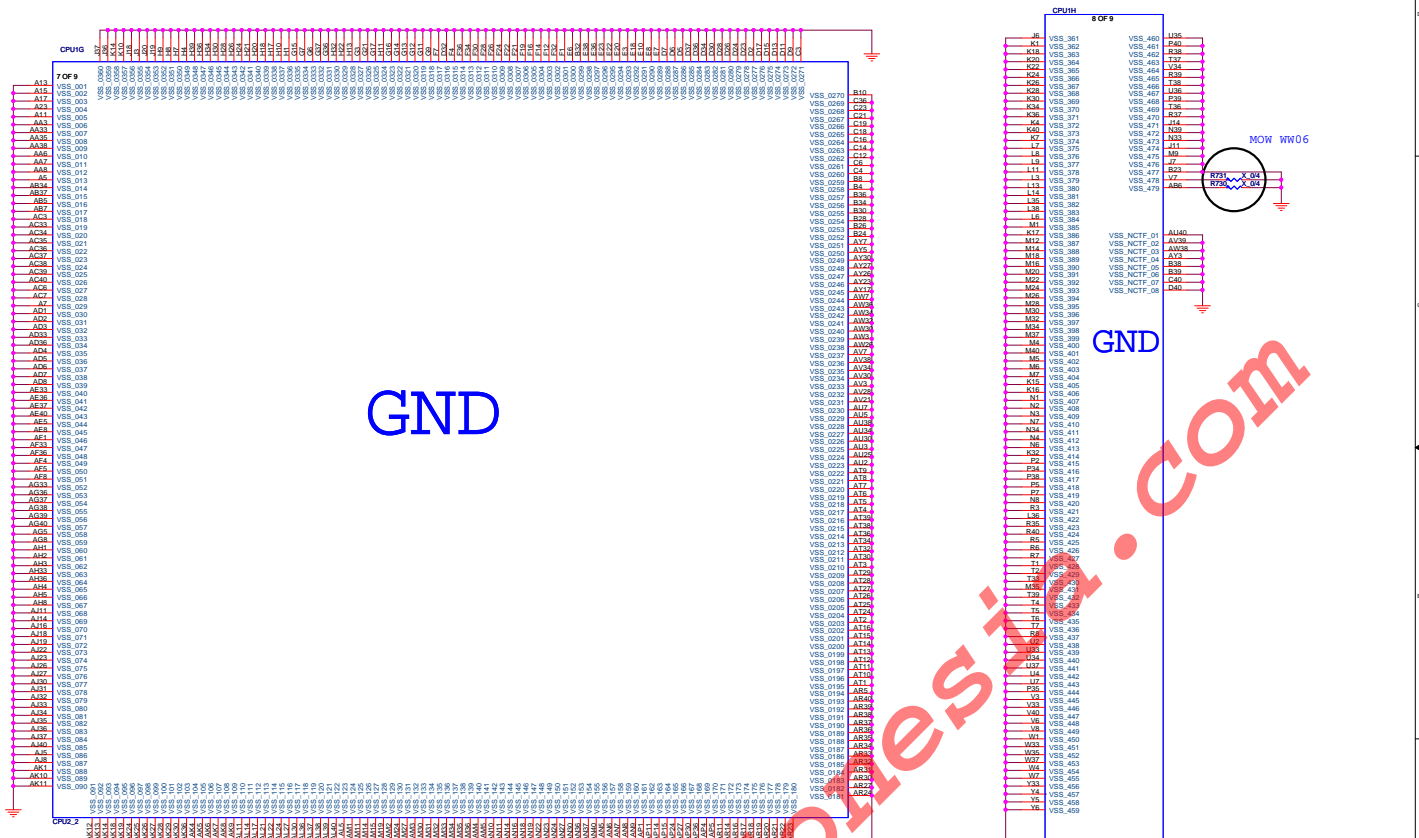
 MICRO-START INTL CO.,LTD.	
File: Cover Sheet	
Size: MS-7837	Rev: 1.0
Date: Thursday, December 13, 2012 Sheet: 1 of 36	

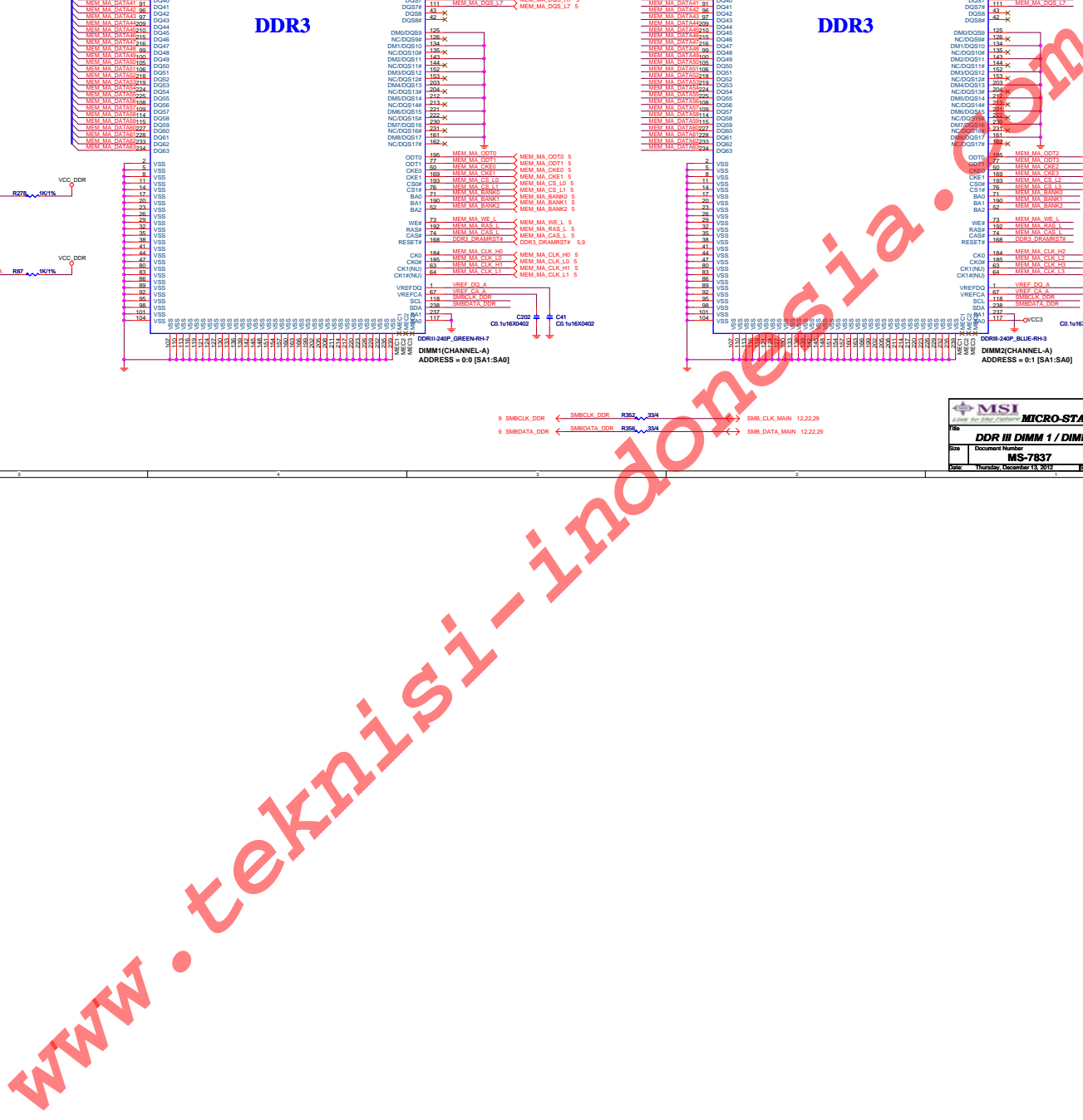


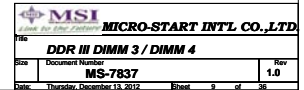








DDRIII DIMM_A2

DDRIII DIMM_B2

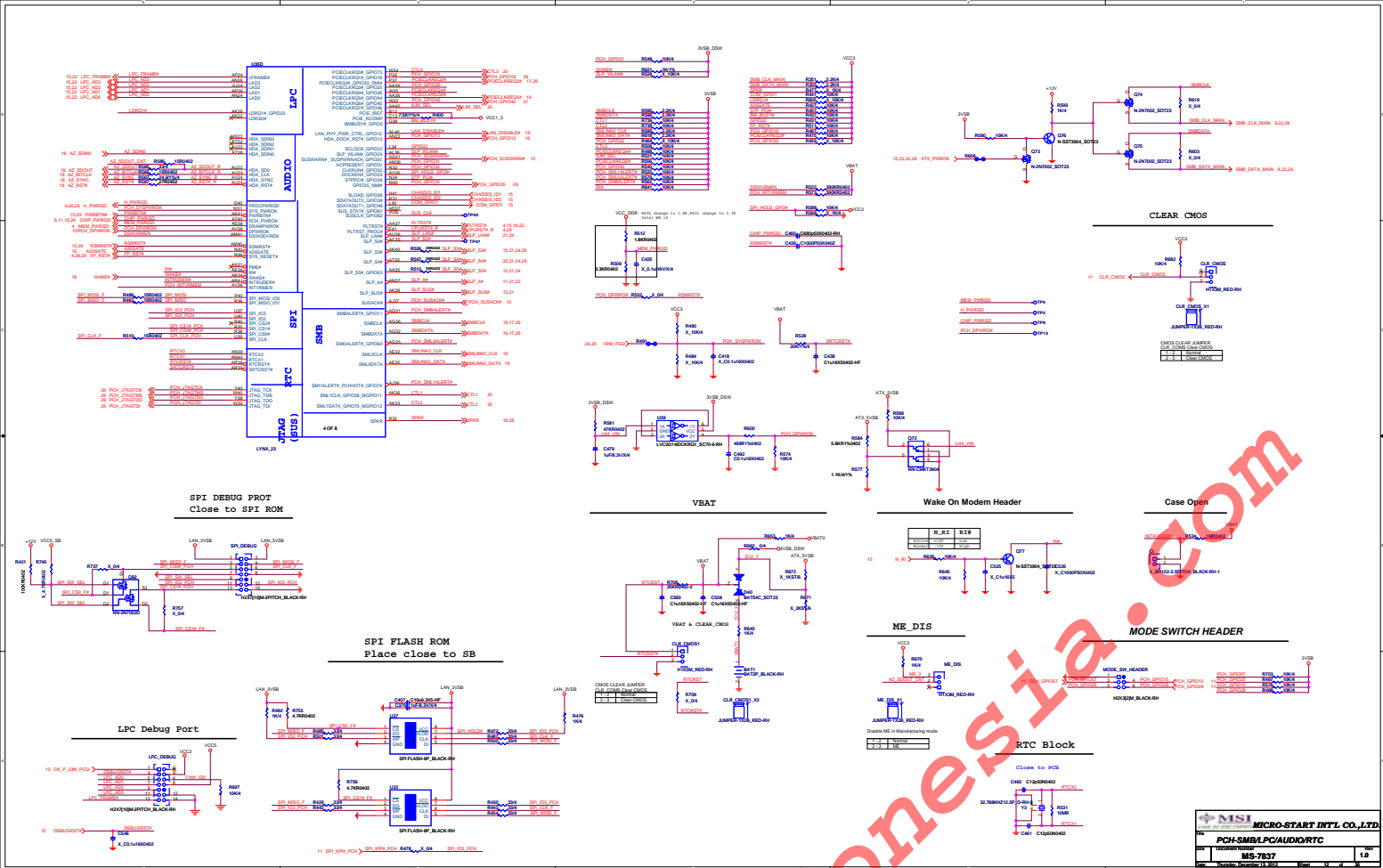


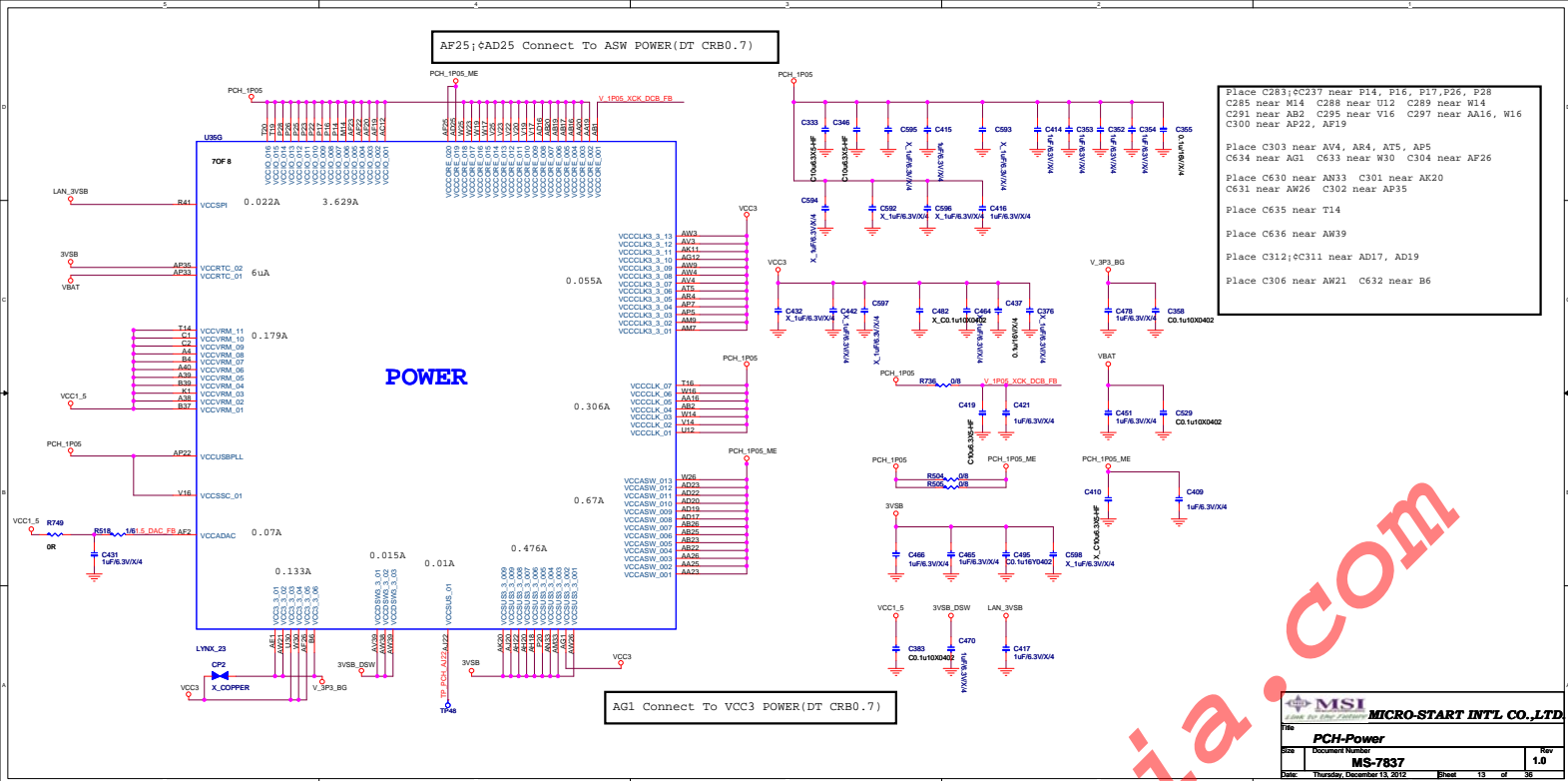
BIOS STARAPS

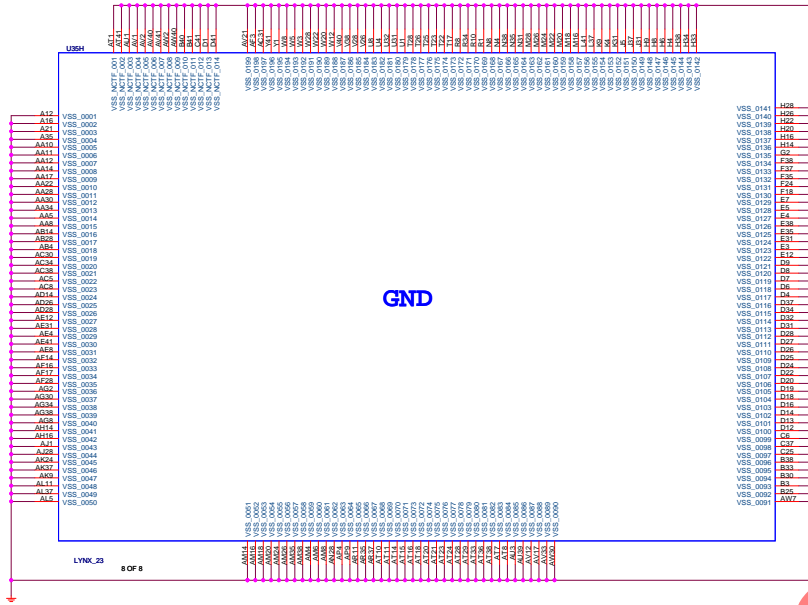
BIOS Device Select

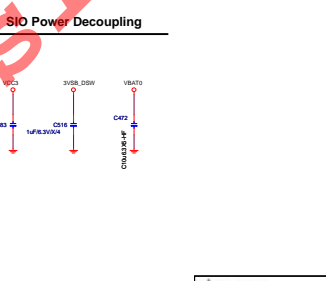
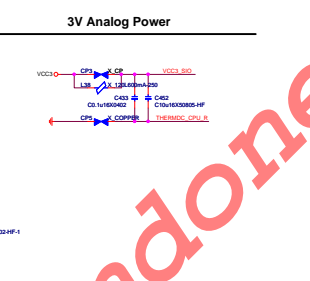
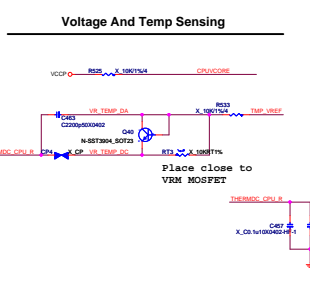
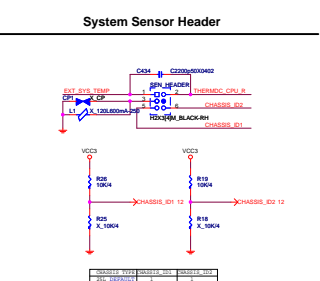
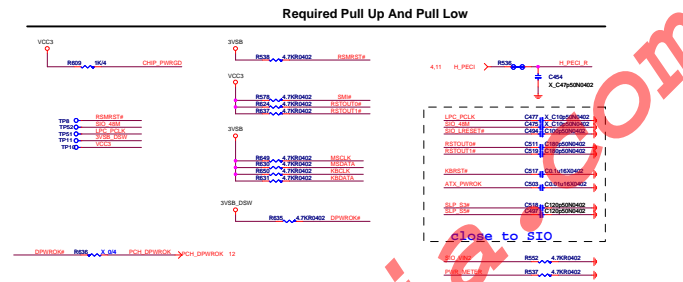
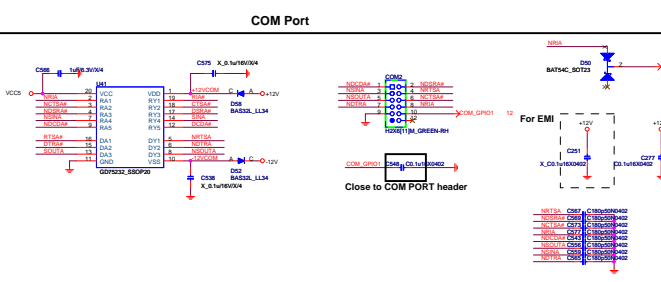
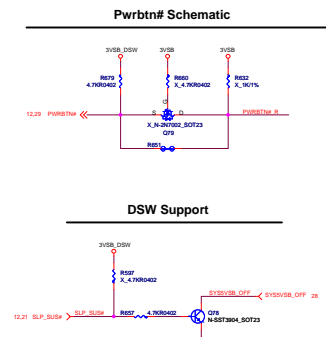
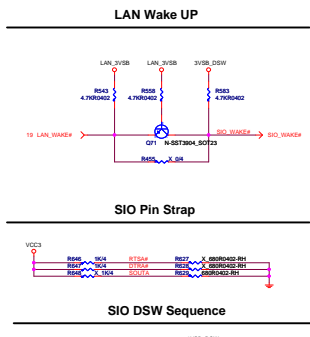
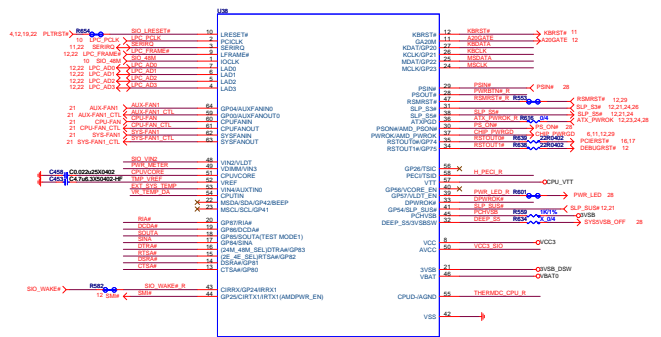
NA	0	0
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SPI	1	1
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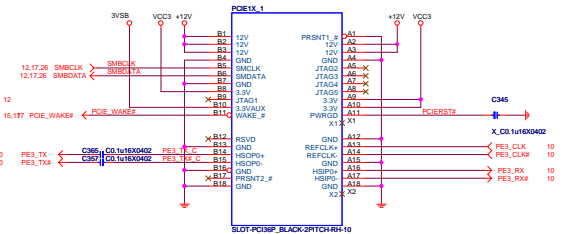


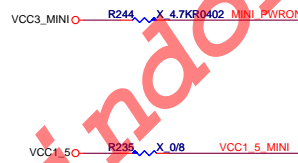
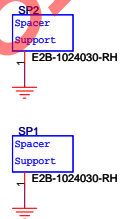
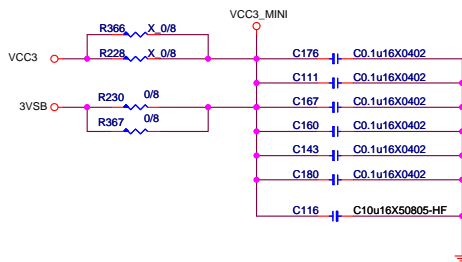




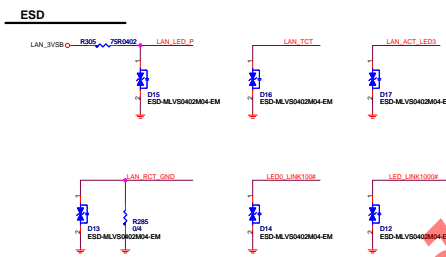
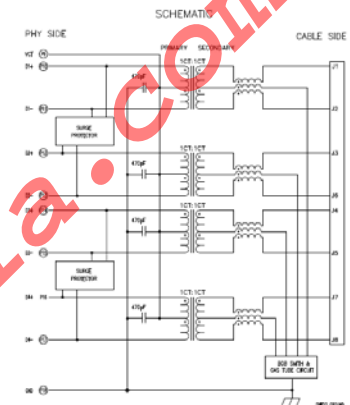


PCI EXPRESS x1-PORT

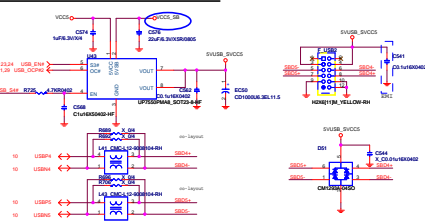
[illegible]



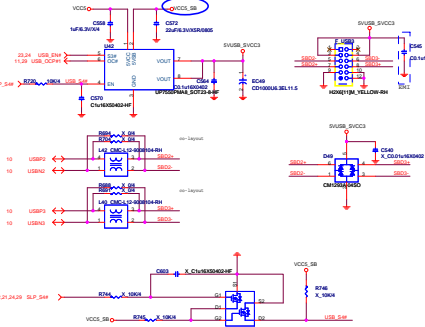
For EMI
R551 & R544 Please near to lan connector



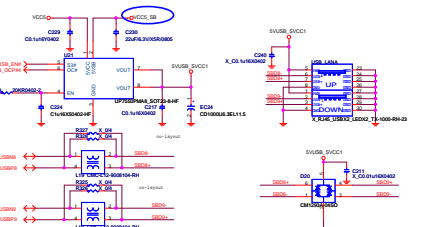
Front Panel USB Connector For USB Port 6 / 7



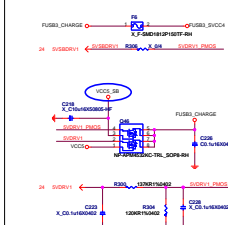
Front Panel USB Connector For USB Port 2 / 3



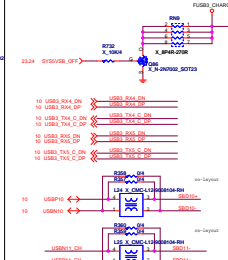
Rear USB Connector For USB Port 8 / 9



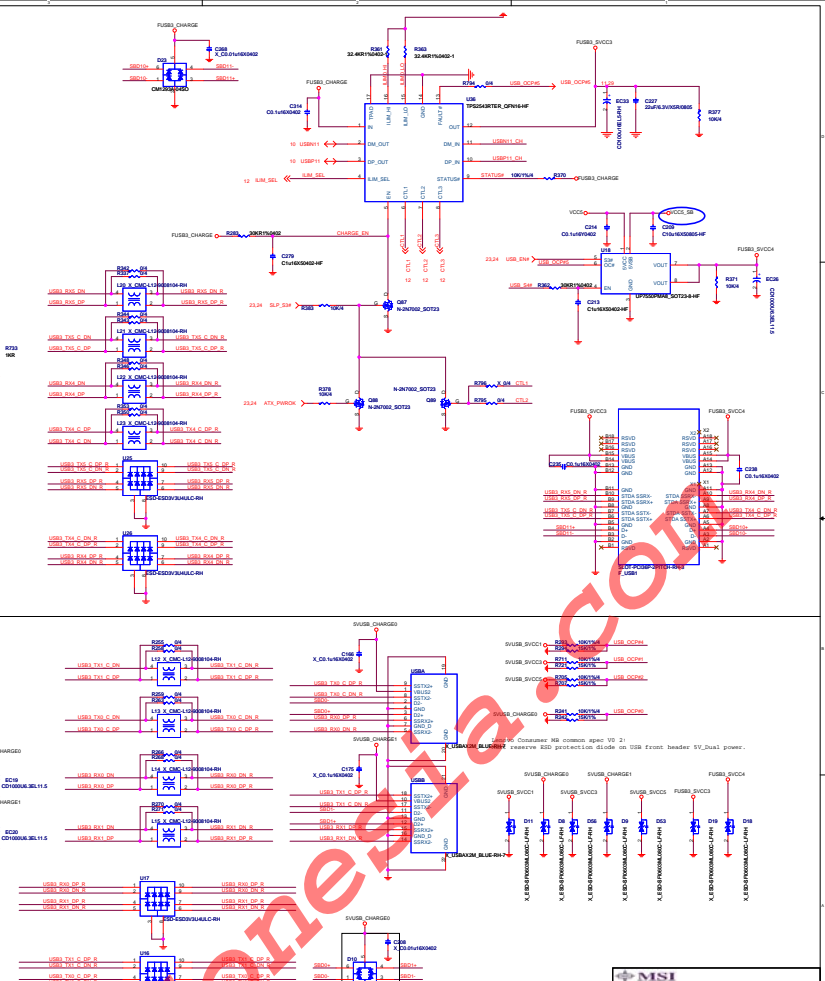
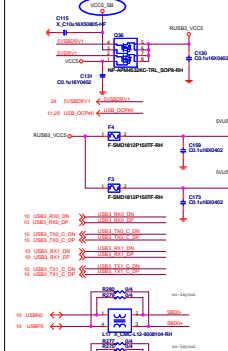
Front Panel USB Connector For USB Port 10 / 11



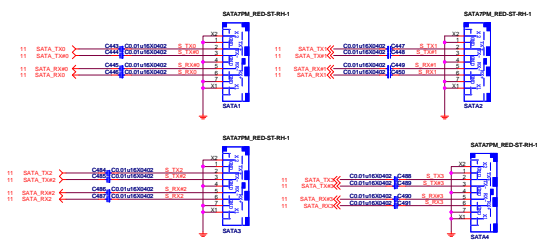
USB charger port power discharge circuit



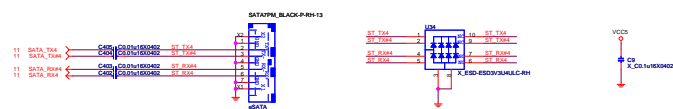
Rear USB Connector For USB Port 0 / 1



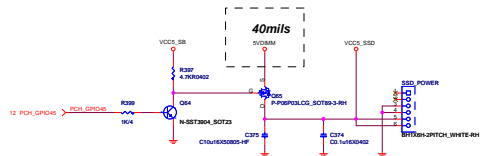
CD Power Header (For Turbo Boot)



ESATA Connector



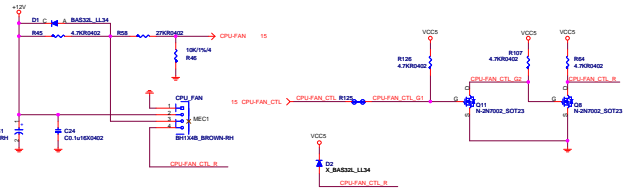
SSD Power Header (For Turbo Boot)



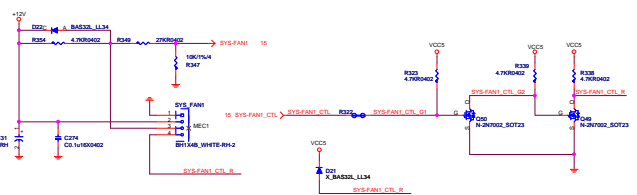
Reserve For Intel VPRO Test



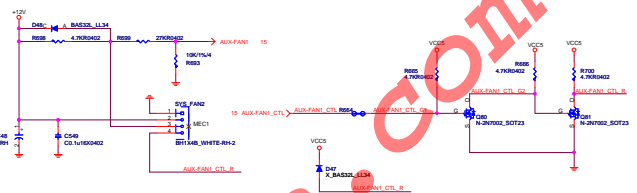
CPU Fan

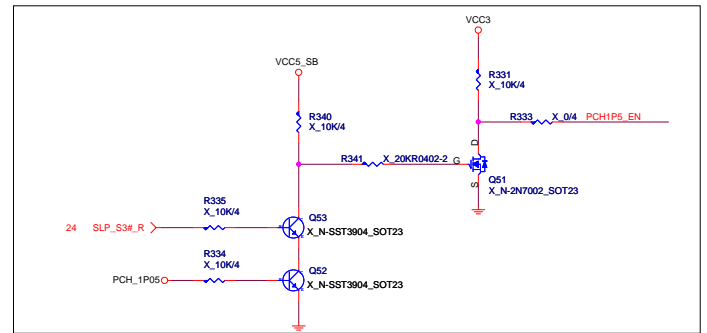


System Fan



Power Fan

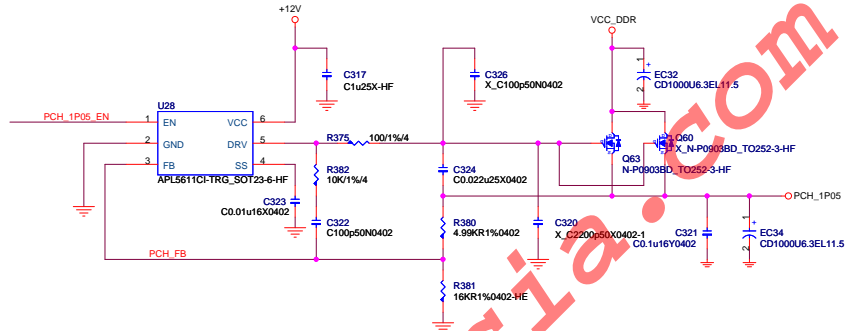
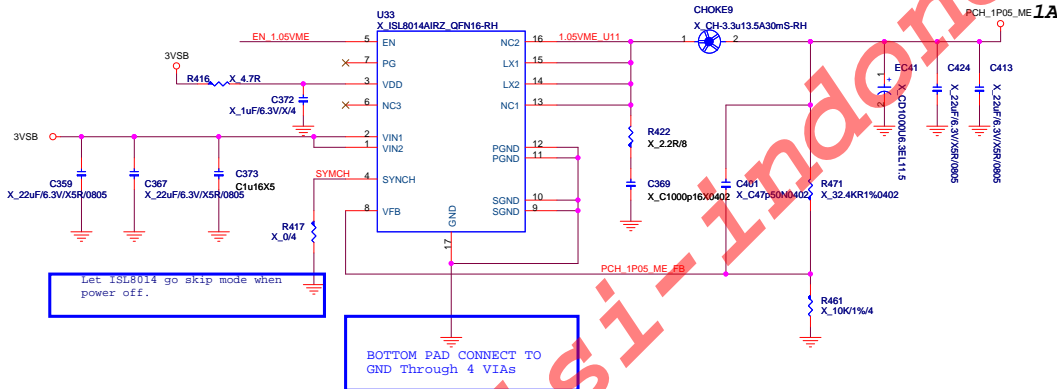


$$V_{out} = 0.8[(R_{336} + R_{332}) / R_{332}] = 1.509V$$


PCH Core Power

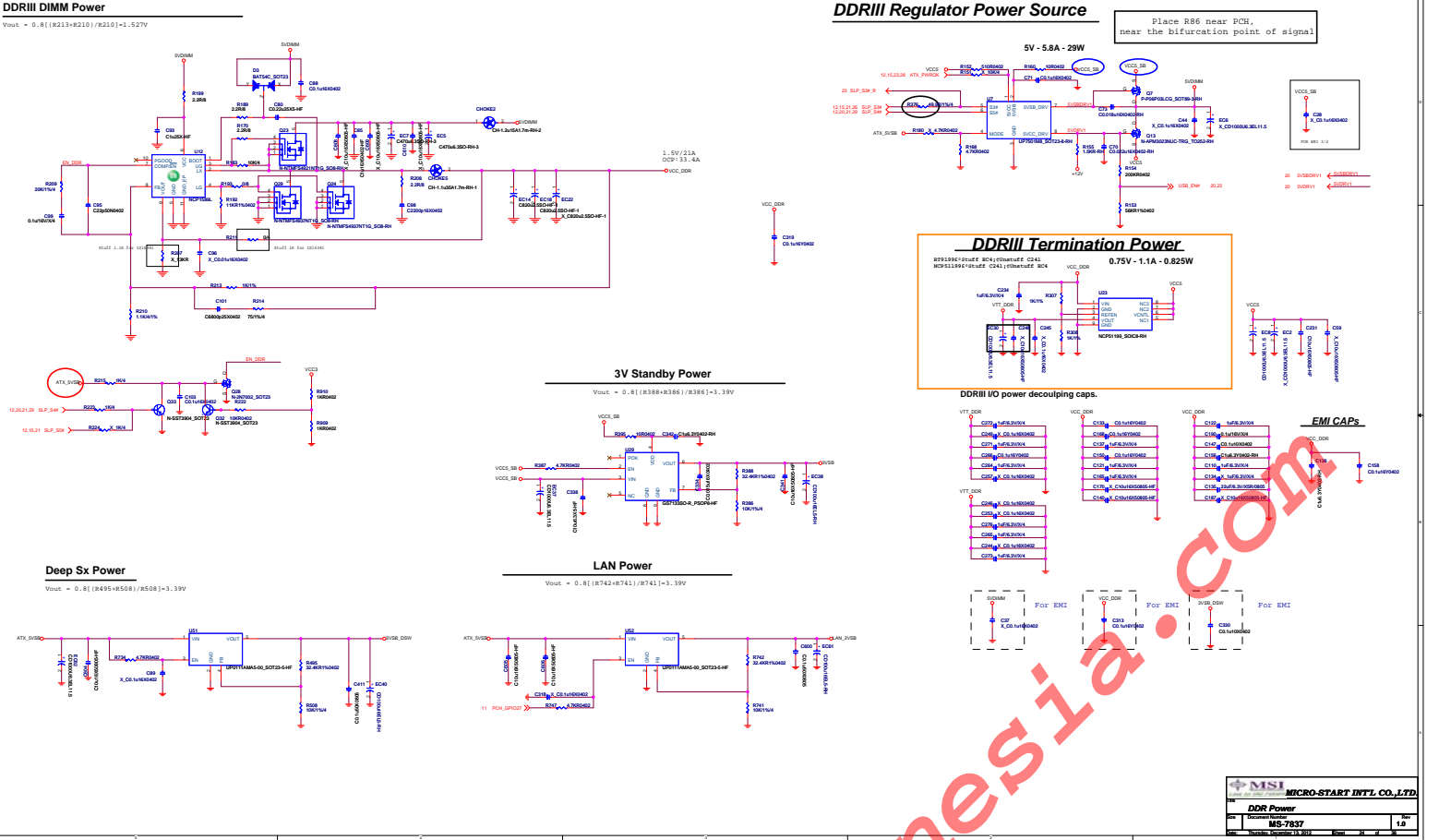
sequence requirement on VCC1_5 and PCH_1P05

$$V_{out} = 0.8[(R_{380} + R_{381})/R_{381}] = 1.0495V$$


$$V_{out} = 0.8[(R_{471}+R_{461})/R_{461}]=1.0495V$$


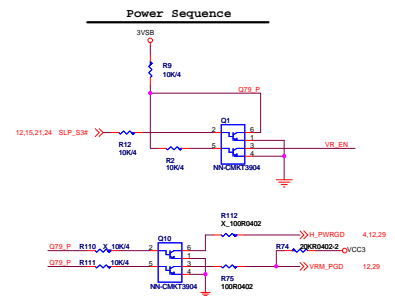
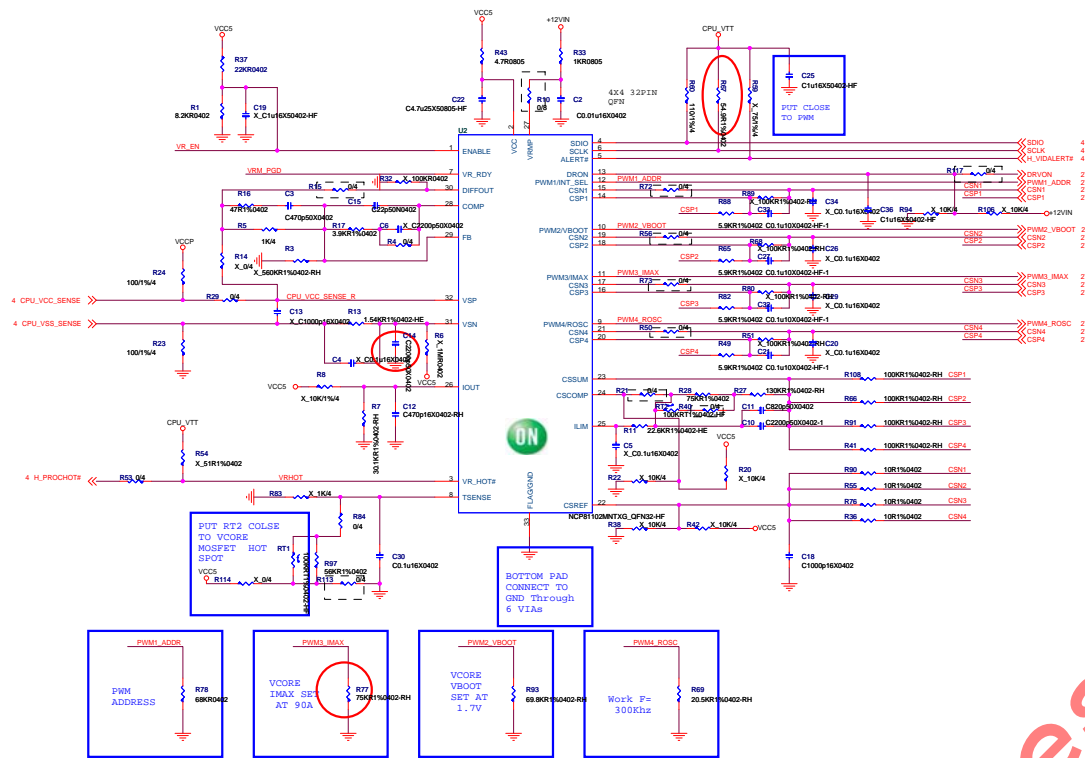
ME Power Control

The schematic diagram illustrates the ME Power Control circuit. It features a 3VSB power source connected to a network of resistors (R459, R435, R426, R436), capacitors (C393, C380, C389), and transistors (Q70, Q68). The output is labeled EN_1.05VME. A signal input 11.12.21 SLP_A# is connected to the base of Q70 through resistor R474. The circuit is designed to control the ME power supply.



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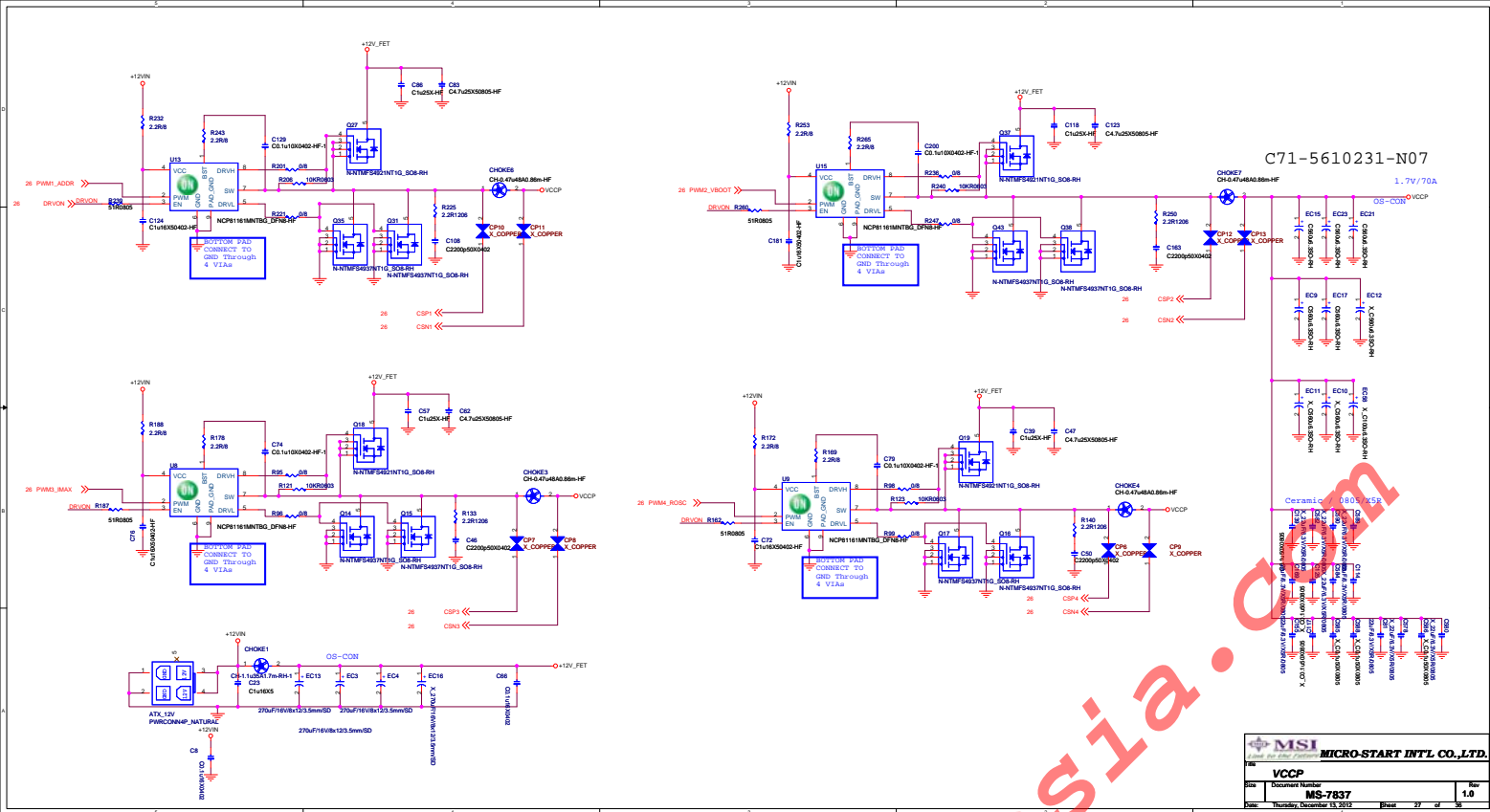
SharkBay VR12.5 Power Circuit - 4 Phase



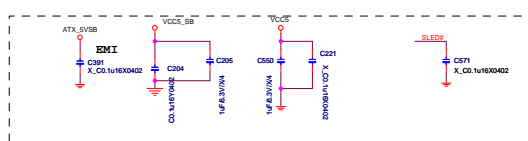
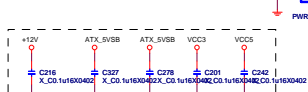
Rosc	Freq.	Rosc	Freq.	Rosc	Freq.	Rosc	Freq.	Rosc	Freq.
10K	250KHz	20.9K	340KHz	61.9K	430KHz	105K	520KHz	165K	610KHz
12K	260KHz	34K	350KHz	64.9K	440KHz	110K	530KHz	174K	620KHz
14K	270KHz	36.5K	360KHz	69.8K	450KHz	115K	540KHz	182K	630KHz
16.2K	280KHz	40.2K	370KHz	73.2K	460KHz	121K	550KHz	191K	640KHz
18.2K	290KHz	43.2K	380KHz	76.7K	470KHz	130K	560KHz	200K	650KHz
20.5K	300KHz	46.4K	390KHz	82.5K	480KHz	137K	570KHz		
23.2K	310KHz	49.9K	400KHz	88.7K	490KHz	143K	580KHz		
25.5K	320KHz	53.6K	410KHz	93.1K	500KHz	150K	590KHz		
28K	330KHz	57.6K	420KHz	100K	510KHz	158K	600KHz		

PWM ADDRESS	
RESISTOR VALUE	SVID ADDRESS FOR VOORE RAIL
10K	0000
25K	0010
45K	0100
70K	0110
95K	1000
125K	1010
165K	1100

BOOT VOLTAGE & Phase no.		
RESISTOR VALUE	BOOT VOLTAGE	Phase no.
30.1K	1.5V	1
49.9K	1.65V	2
69.8K	1.8V	3
90K	1.75V	1
130K	1.0V	2
150K	1.65V	2
155K	1.7V	2
Open	1.75V	2

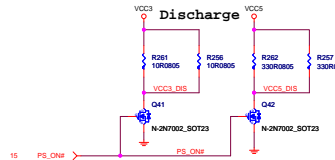
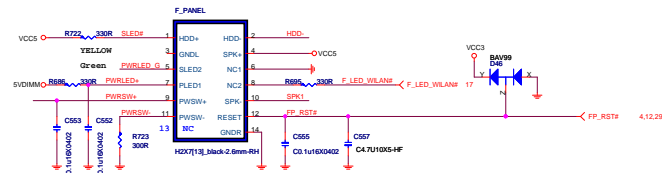
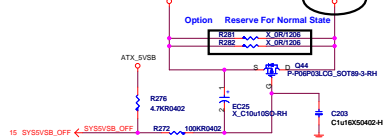


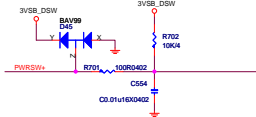
24 Pin ATX Power Connector

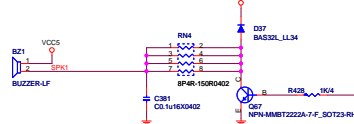


Tune ATX_5VSB inrush current to 2A from 4A

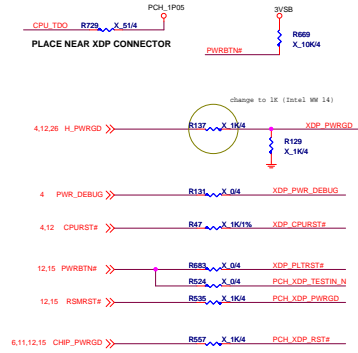
Tune ATX_5VSB inrush current to 2A from 4A





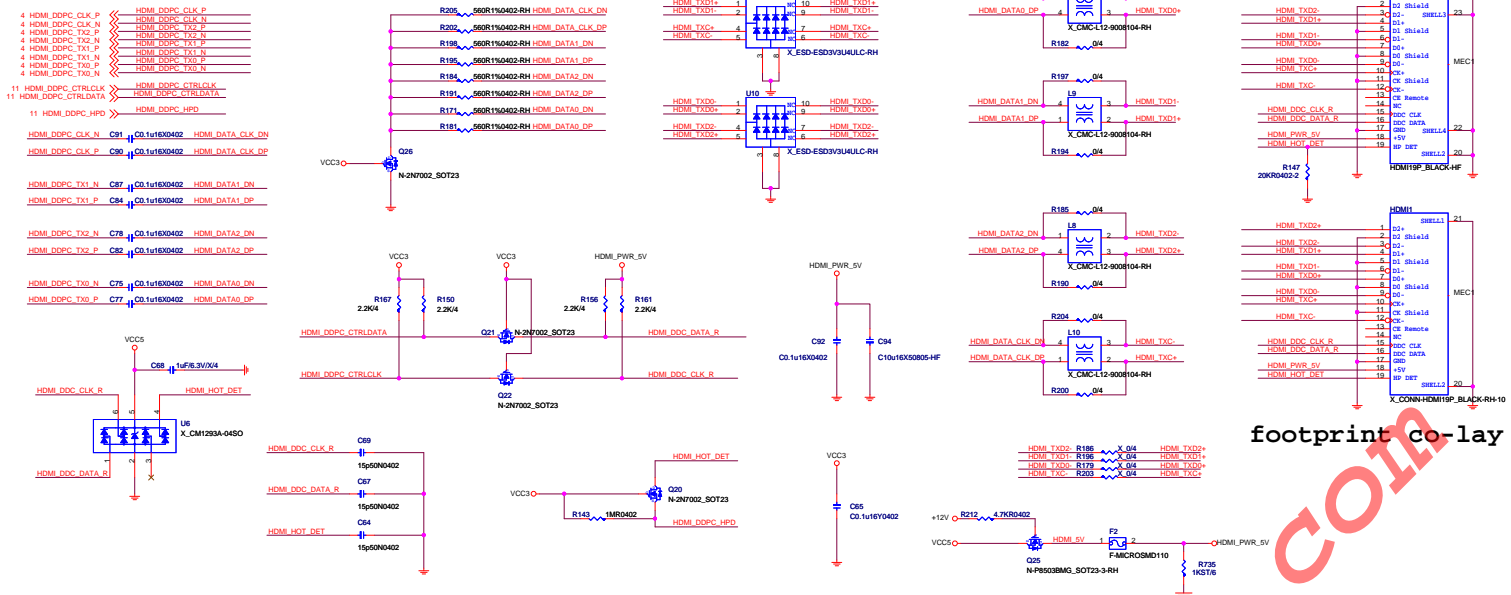


CHU_VTT	JXDPI			
	3	VCC_OBS_AB	TK01	55
	4	VCC_OBS_CD	TK00	57
	5		TK03	52
	6		TRST#	56
	7		TMS	58
H-CE00	9	OBFSN_0_A		
H-CE01	10	OBFSN_0_A	HO0K0	39
H-CE02	11	OBFSN_0_A	HO0K1	41
H-CE03	12	OBFSN_0_A	HO0K2	43
	13	OBFSN_0_B	HO0K3	45
	14	OBFSN_0_B	HO0K4	47
H-CE04	15	OBFSN_0_B	TPCLK#_H00K1	44
H-CE05	16	OBFSN_0_B	TPCLK#_H00K2	46
H-CE06	17	OBFSN_0_B	TPCLK#_H00K3	48
H-CE07	18	OBFSN_0_B	TPCLK#_H00K4	50
H-CE08	19	OBFSN_0_B	TPCLK#_H00K5	52
H-CE09	20	OBFSN_0_B	TPCLK#_H00K6	54
H-CE10	21	OBFSN_0_B	TPCLK#_H00K7	56
H-CE11	22	OBFSN_0_B	TPCLK#_H00K8	58
H-CE12	23	OBFSN_0_B	TPCLK#_H00K9	60
H-CE13	24	OBFSN_0_B	TPCLK#_H00K10	62
H-CE14	25	OBFSN_0_B	TPCLK#_H00K11	64
H-CE15	26	OBFSN_0_B	TPCLK#_H00K12	66
H-CE16	27	OBFSN_0_B	TPCLK#_H00K13	68
H-CE17	28	OBFSN_0_B	TPCLK#_H00K14	70
H-CE18	29	OBFSN_0_B	TPCLK#_H00K15	72
H-CE19	30	OBFSN_0_B	TPCLK#_H00K16	74
H-CE20	31	OBFSN_0_B	TPCLK#_H00K17	76
H-CE21	32	OBFSN_0_B	TPCLK#_H00K18	78
H-CE22	33	OBFSN_0_B	TPCLK#_H00K19	80
H-CE23	34	OBFSN_0_B	TPCLK#_H00K20	82
H-CE24	35	OBFSN_0_B	TPCLK#_H00K21	84
H-CE25	36	OBFSN_0_B	TPCLK#_H00K22	86
H-CE26	37	OBFSN_0_B	TPCLK#_H00K23	88
H-CE27	38	OBFSN_0_B	TPCLK#_H00K24	90
H-CE28	39	OBFSN_0_B	TPCLK#_H00K25	92
H-CE29	40	OBFSN_0_B	TPCLK#_H00K26	94
H-CE30	41	OBFSN_0_B	TPCLK#_H00K27	96
H-CE31	42	OBFSN_0_B	TPCLK#_H00K28	98
H-CE32	43	OBFSN_0_B	TPCLK#_H00K29	100
H-CE33	44	OBFSN_0_B	TPCLK#_H00K30	102
H-CE34	45	OBFSN_0_B	TPCLK#_H00K31	104
H-CE35	46	OBFSN_0_B	TPCLK#_H00K32	106
H-CE36	47	OBFSN_0_B	TPCLK#_H00K33	108
H-CE37	48	OBFSN_0_B	TPCLK#_H00K34	110
H-CE38	49	OBFSN_0_B	TPCLK#_H00K35	112
H-CE39	50	OBFSN_0_B	TPCLK#_H00K36	114
H-CE40	51	OBFSN_0_B	TPCLK#_H00K37	116
H-CE41	52	OBFSN_0_B	TPCLK#_H00K38	118
H-CE42	53	OBFSN_0_B	TPCLK#_H00K39	120
H-CE43	54	OBFSN_0_B	TPCLK#_H00K40	122
H-CE44	55	OBFSN_0_B	TPCLK#_H00K41	124
H-CE45	56	OBFSN_0_B	TPCLK#_H00K42	126
H-CE46	57	OBFSN_0_B	TPCLK#_H00K43	128
H-CE47	58	OBFSN_0_B	TPCLK#_H00K44	130
H-CE48	59	OBFSN_0_B	TPCLK#_H00K45	132
H-CE49	60	OBFSN_0_B	TPCLK#_H00K46	134
H-CE50	61	OBFSN_0_B	TPCLK#_H00K47	136
H-CE51	62	OBFSN_0_B	TPCLK#_H00K48	138
H-CE52	63	OBFSN_0_B	TPCLK#_H00K49	140
H-CE53	64	OBFSN_0_B	TPCLK#_H00K50	142
H-CE54	65	OBFSN_0_B	TPCLK#_H00K51	144
H-CE55	66	OBFSN_0_B	TPCLK#_H00K52	146
H-CE56	67	OBFSN_0_B	TPCLK#_H00K53	148
H-CE57	68	OBFSN_0_B	TPCLK#_H00K54	150
H-CE58	69	OBFSN_0_B	TPCLK#_H00K55	152
H-CE59	70	OBFSN_0_B	TPCLK#_H00K56	154
H-CE60	71	OBFSN_0_B	TPCLK#_H00K57	156
H-CE61	72			

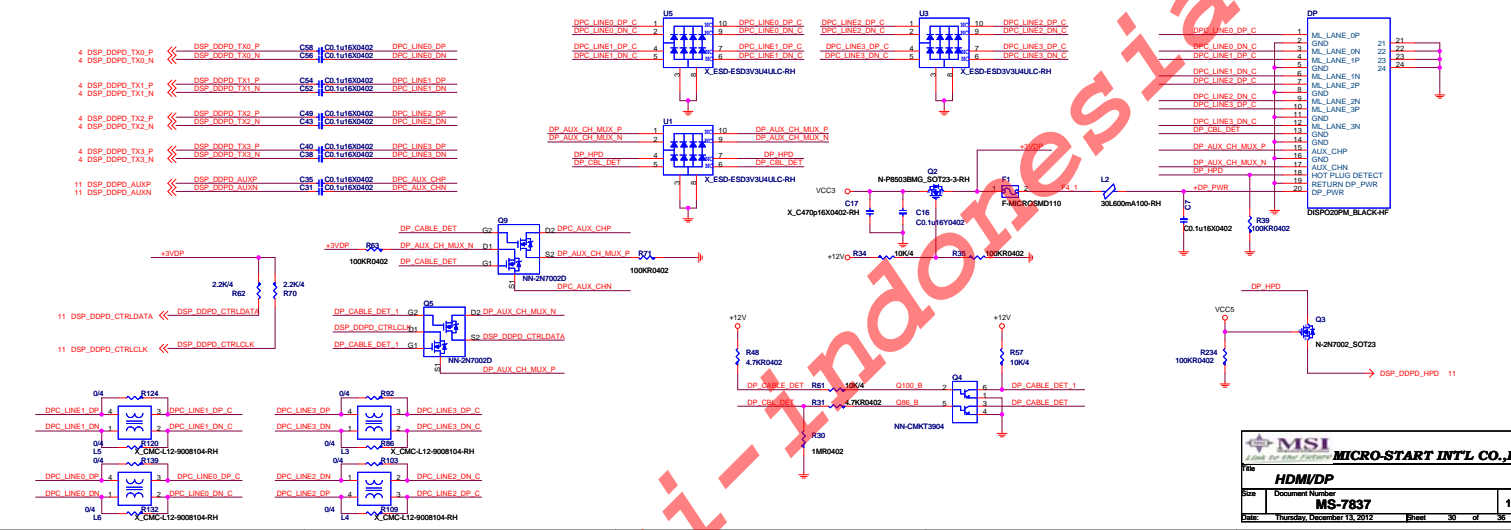


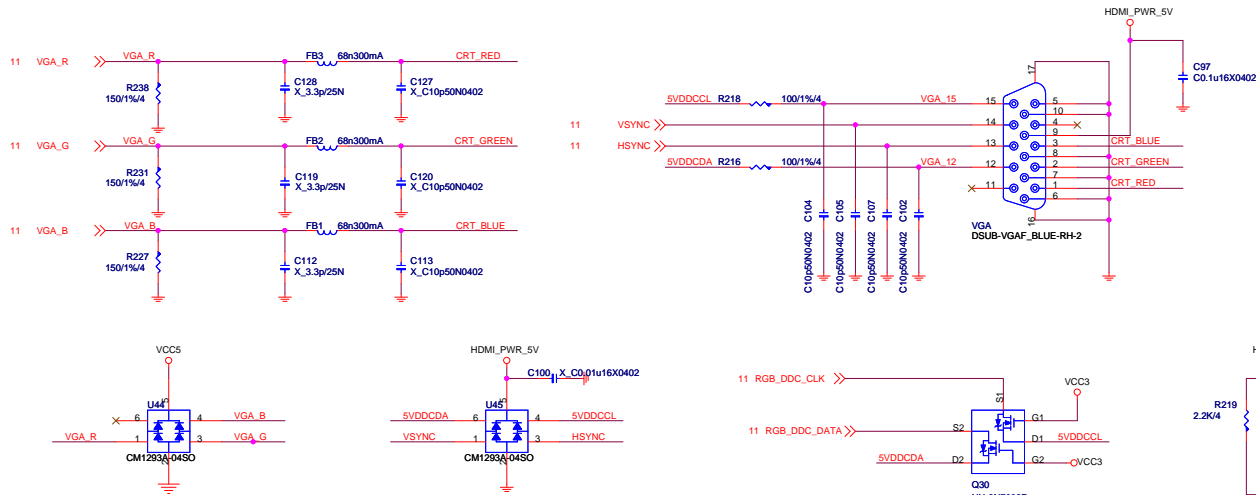
Pin 1 to 59 of the XTB1605P-RH component. The diagram shows a top-down view of the component with pins numbered 1 to 59. Pin 1 is labeled 'PCH_GPIO21' and Pin 59 is labeled 'PCH_GPIO35'. The component is labeled 'XTB1605P-RH' at the bottom. A large red watermark '012' is overlaid on the diagram.

Pin	Signal	Pin	Signal	Pin	Signal
1	PCH_GPIO21	17	BP1M1_06/TP_13	33	SIO_P1ME2
2	PCH_GPIO19	18	BP1M1_16/TP_12	34	USB_OCPR6
3	PCH_GPIO20	19	BP1M1_28/TP_11	35	USB_OCPR4
4	PCH_GPIO18	20	BP1M1_36/TP_10	36	USB_OCPR2
5	PCH_GPIO17	21	BP1M1_44	37	USB_OCPR1
6	PCH_GPIO16	22	BP1M1_52	38	USB_OCPR0
7	PCH_GPIO15	23	BP1M1_60	39	
8	PCH_GPIO14	24	BP1M1_68	40	
9	PCH_GPIO13	25	BP1M1_76	41	
10	PCH_GPIO12	26	BP1M1_84	42	
11	PCH_GPIO11	27	BP1M1_92	43	
12	PCH_GPIO10	28	BP1M1_100	44	Q19/SB
13	PCH_GPIO09	29	BP1M1_108	45	
14	PCH_GPIO08	30	BP1M1_116	46	
15	PCH_GPIO07	31	BP1M1_124	47	
16	PCH_GPIO06	32	BP1M1_132	48	
17	PCH_GPIO05	33	BP1M1_140	49	
18	PCH_GPIO04	34	BP1M1_148	50	
19	PCH_GPIO03	35	BP1M1_156	51	
20	PCH_GPIO02	36	BP1M1_164	52	
21	PCH_GPIO01	37	BP1M1_172	53	
22	PCH_GPIO00	38	BP1M1_180	54	
23	PCH_GPIO00	39	BP1M1_188	55	
24	PCH_GPIO00	40	BP1M1_196	56	
25	PCH_GPIO00	41	BP1M1_204	57	
26	PCH_GPIO00	42	BP1M1_212	58	
27	PCH_GPIO00	43	BP1M1_220	59	
28	PCH_GPIO00	44	BP1M1_228		
29	PCH_GPIO00	45	BP1M1_236		
30	PCH_GPIO00	46	BP1M1_244		
31	PCH_GPIO00	47	BP1M1_252		
32	PCH_GPIO00	48	BP1M1_260		
33	PCH_GPIO00	49	BP1M1_268		
34	PCH_GPIO00	50	BP1M1_276		
35	PCH_GPIO00	51	BP1M1_284		
36	PCH_GPIO00	52	BP1M1_292		
37	PCH_GPIO00	53	BP1M1_300		
38	PCH_GPIO00	54	BP1M1_308		
39	PCH_GPIO00	55	BP1M1_316		
40	PCH_GPIO00	56	BP1M1_324		
41	PCH_GPIO00	57	BP1M1_332		
42	PCH_GPIO00	58	BP1M1_340		
43	PCH_GPIO00	59	BP1M1_348		
44	PCH_GPIO00				
45	PCH_GPIO00				
46	PCH_GPIO00				
47	PCH_GPIO00				
48	PCH_GPIO00				
49	PCH_GPIO00				
50	PCH_GPIO00				
51	PCH_GPIO00				
52	PCH_GPIO00				
53	PCH_GPIO00				
54	PCH_GPIO00				
55	PCH_GPIO00				
56	PCH_GPIO00				
57	PCH_GPIO00				
58	PCH_GPIO00				
59	PCH_GPIO00				



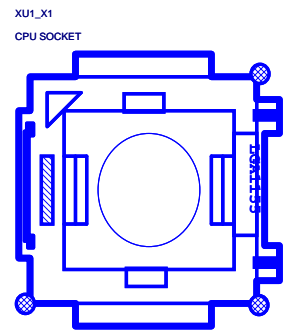
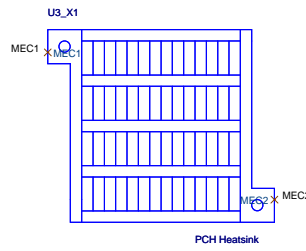
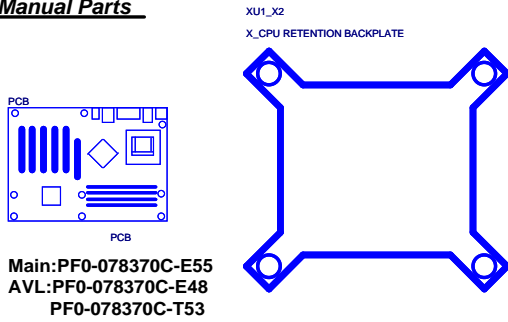
footprint co-lay



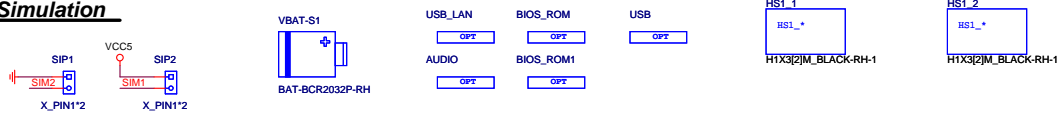


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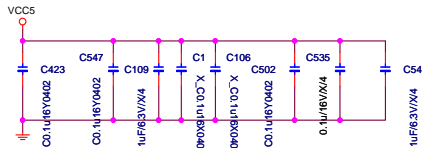
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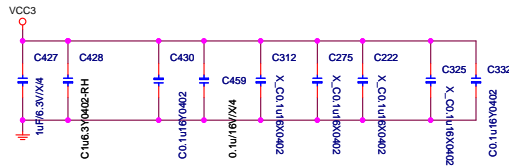
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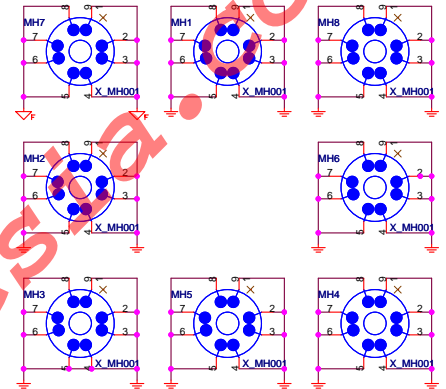
For EMI



For Moat CAP

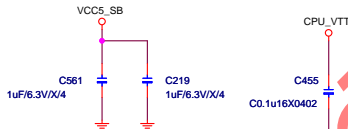
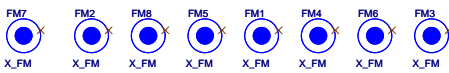


Mounting Holes



Optics Orientation Holes

Optical Fiducial Marks-120



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The block diagram illustrates the system architecture for the Intel LGA1150 Processor. The central component is the **Intel LGA1150 Processor**, which is connected to several other components:

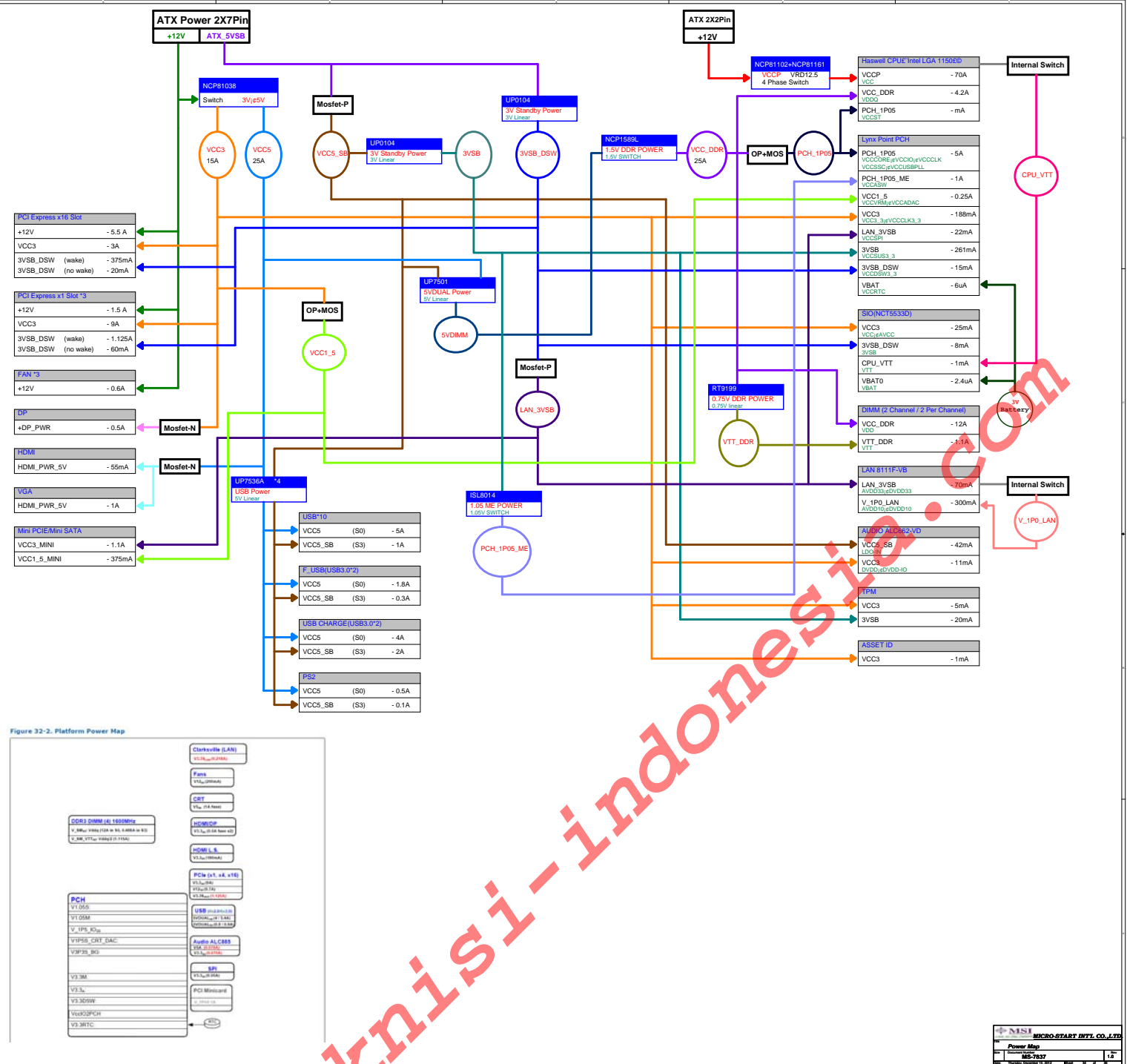
- VR 12.5 NCP61102**: Connected to the processor via **VRM_FMS0** and **VRM_FMS1** signals.
- PCH (Platform Controller Hub)**: The processor is connected to the PCH via **REF_FMS0** and **REF_FMS1** signals. The PCH is also connected to the VR 12.5 NCP61102 via **VRM_FMS0** and **VRM_FMS1** signals.
- Super I/O**: Connected to the PCH via **IO_FMS0** and **IO_FMS1** signals. The Super I/O is also connected to the Front Panel via **FS2B** and **FS2C** signals.
- DDR NCP1589L**: Connected to the PCH via **DDR_FMS0** and **DDR_FMS1** signals. The DDR NCP1589L is also connected to the PCH via **DDR_FMS2** and **DDR_FMS3** signals.
- Power CON**: Connected to the Super I/O via **ATX_FMS0C** and **ATX_FMS1C** signals. The Power CON is also connected to the Super I/O via **ATX_FMS0C** and **ATX_FMS1C** signals.

The diagram shows the interconnections between the processor, the PCH, the Super I/O, the VR 12.5 NCP61102, the DDR NCP1589L, and the Power CON, highlighting the various FMS (Function Module Signal) and FMS (Function Module Signal) signals used for communication.

The diagram illustrates the Intel Atom D2700 SoC at the center, connected to several components:

- Intel 1150 Processor:** Connected via a bidirectional **QPI/DDR3** interface.
- ALC 892 HD Codec:** Connected via an **AL2078** interface.
- RESET SW:** Connected via a **PI2078** interface.
- LAN #111:** Connected via a **PL2078** interface.
- Super I/O NCT5533D:** Connected via a bidirectional **SMbus** interface.
- Storage and Expansion:** The Super I/O NCT5533D is further connected to:
 - PCIe X16 Slot**
 - PCI X1 Slot**
 - MPC101MSATA Slot**

12V
5V
3.3V
5VDRV1
VCC1_5REF
DDR_EN
VCC1_5
VCC_DDR
PCH_1P05
CHIP_PWRGD
MEM_PWRGD
H_PWRGD
VCCCP
FCH_SYSPWROK
SUS_STAT#
PLTSTST#



SIG(CT67790)			
PIN NAME	USAGE	Input/Output	NOTES
GPIO0	ALUX/FAN1_CTL	Output	Fan speed control
GPIO1	NA	NA	NA
GPIO2	NA	NA	NA
GPIO3	NA	NA	NA
GPIO4	ALUX/FAN1	Input	Fan speed sense
GPIO5	ALUX/ANNG2	Input	Pull low
GPIO6	ALUX/ANNG3	Input	Pull low
GPIO7	NA	NA	NA
GPIO8	RTSB	Input	Com port signal
GPIO11	DSBIB	Input	Com port signal
GPIO12	SCUTB	Output	Com port signal
GPIO13	SNB	Input	Com port signal
GPIO14	DTBSB	Output	Com port signal
GPIO15	RTBSB	Output	Com port signal
GPIO16	DSBSB	Input	Com port signal
GPIO17	CTBSB	Input	Com port signal
GPIO20	ADTBA	Input	Keyboard data in
GPIO21	KSCAL	Input	Keyboard clock out
GPIO22	MSDATA	Input	Mouse data in
GPIO23	MSCLK	Output	Mouse clock out

SIO[NC6779D]			
Pin Name	Usage	Input/Output	Notes
GPIO24	SIO_WANENR_R	Output	Wake up signal from LAN
GPIO25	AMDPWR_EN	Input	Pin strap which disabled AMD power sequence
GPIO26	NA	NA	NA
GPIO27	MLEDV	Output	Pull high
GPIO30	RESETCONR	Input	Pull high
GPIO31	SDA_SIO	Output	Reserved GPIO for future use
GPIO32	SCI_SIO	Output	Reserved GPIO for future use
GPIO33	NA	NA	NA
GPIO34	PRSTR	Output	LPT signal
GPIO35	PRSTRDI	Output	LPT signal
GPIO36	PRSTRR	Output	LPT signal
GPIO40	TEST_MODE_EN	Input	Pin strap which disabled test mode
GPIO41	PRINTNR	Output	LPT signal
GPIO42	LPT_SLine	Output	LPT signal
GPIO43	FRACKR	Input	LPT signal
GPIO44	FRACKR	Input	LPT signal
GPIO45	PRSTR	Input	LPT signal
GPIO46	PRSTRLT	Input	LPT signal
GPIO47	RESETCONR	Input	Pull high
GPIO50	SLEWWARNR	Output	DSW signal

[PINQCT6779D]			
PIN NAME	USAGE	Input/Output	NOTES
GP051	SIO_5VDDM	Input	D5W signal
GP052	SUBACK0	Output	D5W signal
GP053	NA	NA	NA
GP054	SLP_S0B5	Input	D5W signal
GP055	SYSSW0_OFF0_R	Output	D5W signal
GP056	PS2_DeT8	Input	PS2 detect signal
GP057	PKW_LED_0	Output	Power led
GP060	RND0	IO	LPT signal
GP061	RND1	IO	LPT signal
GP062	RND2	IO	LPT signal
GP063	RND3	IO	LPT signal
GP064	RND4	IO	LPT signal
GP065	RND5	IO	LPT signal
GP066	RND6	IO	LPT signal
GP067	RND7	IO	LPT signal
GP070	CS0_B0	Output	Pin control which enables D5W
GP071	CS0_GP1	Output	Reserved GPIO for future use
GP072	CS0_GP2	Output	Reserved GPIO for future use
GP073	CS0_GP3	Output	Reserved GPIO for future use
GP074	WDT0_T0R	Output	PCIE reset signal

SQ(NCT6790)			
PIN NAME	USAGE	Input/Output	NOTES
GPIO75	RTSTOUT1#	Output	LPC_Debug card reset signal
GPIO76	RTSTOUT2#	Output	TPM reset signal
GPIO80	CTS#A	Input	COM port signal
GPIO81	DSRA#A	Input	COM port signal
GPIO82	RTSA#	Output	COM port signal
GPIO83	DTRA#	Output	COM port signal
GPIO84	SINA	Input	COM port signal
GPIO85	SOUTA	Output	COM port signal
GPIO86	DCDA#	Input	COM port signal
GPIO87	RIA#	Input	COM port signal